REMARKS

Status of the Claims:

Claims 3, 5, and 11 have been amended. Claims 12-14 have been added. After amending the claims as set forth above, claims 1-3, 5, 7, 8, and 10-14 are now pending in this application.

I. Claim Objection

Claim 5 is objected to as being in improper form because a multiple dependent claim cannot depend from any other multiple dependent claim. Applicant has amended claim 5 to depend on claim 1 (and added new claims having the features of claim 5 that depend on claims 2 and 3). Accordingly, Applicant respectfully requests that the objection be withdrawn.

II. Claim Rejections – 35 U.S.C. § 103

A. The Sakamoto Reference

Claims 1, 2, 3, 7, and 8 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto (Pub. No. US 2002/0024114 A1). These rejections are respectfully traversed in view of the claims as amended herein.

Independent claim 1 recites a bipolar transistor suitable for operation as a saturated switch, the bipolar transistor comprising:

> a first semiconductor region of a first conductivity type defining a collector region;
>
> a second semiconductor region of a second conductivity type defining a base region;
>
> a third semiconductor region of said first conductivity type defining a emitter region; and
>
> a metal layer providing contacts to said base and emitter regions;
>
> wherein the emitter region defines a first surface, the base region extending to said surface in locations defined by apertures through emitter region, said metal layer overlying said first surface,
>
> wherein the bipolar transistor has a specific area resistance less than 500mOhms.mm^2,
>
> and wherein the thickness of said metal layer is greater than 3μm.

Sakamoto, alone or in the combination suggested by the Examiner, does not teach, suggest, or render predictable a transistor, as recited in claim 1, including these features.

As described in the specification, claim 1 provides a benefit of reduced saturation voltage for bipolar transistors which would already have a specific area resistance less than 500 mOhms.mm^2 with conventional metallization thickness. Specifically, as explained in the specification, the small reduction in voltage drop along the metal contact tracks gives rise to more uniform biasing of the emitter/base junction so that all of the active part of the transistor is switched on, resulting in a more efficient use of the silicon area. *See* Specification at p. 6 ll. 5-8. This leads to a disproportionately large reduction in the voltage drop across the collector/emitter junction when this is operated in the saturation region, and so leading to a disproportionately large reduction in specific area resistance. *See id.* Indeed, as described in the specification, the resulting reduction in voltage drop across the device may be around 30%. *See id.* at p. 6 ll. 5-30. This reduction is **in contrast to the 2% that might have been expected** (as discussed later) from a change in metal layer thickness from 2 microns to 6 microns.

According to the Examiner, Sakamoto discloses:

> a bipolar transistor suitable for operation as a saturated switch comprising: a first semiconductor region of a first conductivity type defining a collector region (see Fig. 1a, n collector region 21); a second semiconductor region of a second conductivity type defining a base region (see Fig. 1a, p base region 22); a third semiconductor region of said first conductivity type defining a emitter region (see Fig. 1a, n emitter region 24); and a metal layer providing contacts to said base and emitter regions (see Fig. 1a, metal layer 26+27 provided); wherein the emitter region defines a first surface, the base region extending to said surface in locations defined by apertures through emitter region, said metal layer overlying said first surface (see Fig. 1a, emitter region 24 with first surface, base region extended through apertures through emitter region, metal layer from 26+27), wherein the bipolar transistor has a specific area resistance less than 500mOhms.mm2 (see Remarks dated 10/19/2009, page 7, second paragraph, with the matrix design, possible to attain specific area resistance less than 500 mOhms.mm2)

See Office Action at Section 7.

As acknowledged by the Examiner, Sakamoto does not disclose that "the thickness of said metal layer is greater than 3 microns." *See id.* As a result, the Examiner notes that "it would have been obvious to one of ordinary skill to determine the optimum thickness (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237)."

However, the mere presence of the stripe structure or multi-base structure does not inherently make the transistor of Sakamoto suitable for operation as a saturated switch. Nor is there any suggestion in Sakamoto that the device disclosed has been optimized to provide a specific area resistance of less than 500 mOhms.mm^2 – much less a suggestion beyond that of the prior art as laid out in the specification. Sakamoto simply makes no suggestion to one skilled in the art that the saturation performance of the transistor can be improved by increasing the top metal thickness. As such, Sakamoto the Examiner's arguments do not address the recited features of claim 1.

To establish a prima facie obviousness of a claim invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (CCPA 1974). Because Sakamoto and the Examiner's comments do not disclose or suggest the recited features, there can be no prima facie obviousness by seeking to combine these references.

1. The transistor of claim 1 provides unexpected results.

Furthermore, the transistor of claim 1 is not obvious in view of the prior art because it provides unexpected results.

In particular, the devices of the specification have interdigitated or interlocking metal layer contacts arranged to provide electrical contacts to the base and emitter respectively. The skilled person might be aware that the resistance between the opposed ends of a simple block of metal of length L and cross-sectional area A is given by the relationship $R = L/\sigma A$, where R is resistance and σ is the metal conductivity. The skilled person might appreciate that the voltage drop arising from the shaped metal layer of a transistor is not trivally estimated but can be modeled as a resistor network.

In addition, the skilled person might also be aware that increasing the thickness of a metal layer on a transistor would lead to a decrease in the resistance for conduction along the metal

layer, that this reduction in resistance will result in a lower voltage drop along the metal tracks at the operating current condition, and that the metal tracks, which are in the collector-emitter circuit, would result in the same reduction in voltage drop across the collector-emitter terminals of the transistor.

With respect to typical bipolar transistors, the skilled person would also be aware that when operated in the saturation region, the voltage drop across the collector-emitter transistor terminals will typically be, for example, about 31 mV. Through modeling, the contribution to this voltage drop (associated with a 2 micron metal layer, for conduction along the metal tracks) can be determined to be about 1 mV. This modeled data was supplied in the response (dated October 19, 2009), which is herein incorporated by reference in its entirety.

The skilled person might be aware that by thickening the metal layer to, for example, 6 microns, modeling of the voltage drop associated with the metal layer only gives an expected voltage drop of about 0.4mV. In other words, the skilled person **may only expect to reduce the voltage drop (from 1mV) by 0.6mV** in the total voltage drop of 31mV across the device from using a 6 micron layer (instead of a 2 micron layer). That is, the **expected** overall resistance improvement would merely be about 2% from a tripling of the metal track layer thickness. As such, the skilled person may only expect a marginal (2%) improvement by increasing (e.g., tripling) thickness of the metal layer.

Thus, the surprising result is that for transistors in claim 1, **a small reduction** in voltage drop **across the metal contact layer** can also lead to **a very large reduction** in the voltage drop **across the collector/emitter junction of the device**. The reduction in the overall resistance of the transistor does not simply arise from a linear combination of the contact resistance along the metal tracks with the intrinsic device resistance. The unexpected benefit arises from the small change in series track resistance having a disproportionate effect on the collector/emitter saturation voltage.

2. The Industry has had a long-felt need to reduce the effective device resistance.

Saturated switch transistors have been in the market for over 25 years and manufacturers have always desired to reduce the effective device resistance to be as low as possible. However, no one yet has lowered resistance by increasing metal layer thickness for the following reasons.

1) As shown above, the expected benefits from a major increase in metal thickness are minimal; and

2) It is well known in the field of device manufacture that metal layers with thicknesses of greater than about 2 microns, for use as contact:

a) are more costly (because of the amount of metal needed and the process time required for deposition of substantially thicker metal layers);

b) are difficult to align due to the difficulty in seeing the alignment targets beneath the very thick metal layer;

c) are difficult to wet etch due to undercutting; and

d) are difficult to dry etch due to the high component of ion-bombardment required to obtain a near-vertical etch profile eroding the photo-resist before the metal layer is completely etched through. (Simply thickening the resist layer creates critical dimension control issues as it increases the difficulty of obtaining sufficiently controlled photo-exposure over oxide edges.)

Thus, there is prejudice in the art that a metal layer thicker than about 2 microns may be problematic because of increased process difficulties in deposition, alignment, and etch. As such, the inconvenience of extra process time, cost, additional metal use, and etching problems provides no incentive for the person skilled in the field to try using thicker metal layers with expectation of any appreciable overall benefit. Therefore, each and all of these reasons demonstrate that the transistor of claim 1 is not obvious. The fact that no one tried to use this claimed solution in the past three decades, even though the need to reduce device size and power consumption was always a key issue, is clear evidence that the claimed subject matter was not an obvious development.

In summary, (1) the skilled person would not have predicted that an increase in metal thickness, which might possibly be expected to lead to only a small reduction in voltage along metal contact tracks, could lead to such a dramatic reduction in the overall intrinsic resistance of the device; and (2) given the known problems associated with thickening metal layers for contact tracks, the skilled person would have had no incentive to take the costly and time consuming steps associated with doubling or tripling the metal contact layer thickness, given that there was no expectation of any appreciable benefit.

Therefore, for at least the reasons above, claim 1 is not obvious in view of Sakamoto. Thus, claim 1 is allowable. Claims 2, 3, 7, and 8 depend from claim 1 (directly or indirectly) and are allowable for at least the same reasons as claim 1 is allowable. Accordingly, the rejections of claims 1, 2, 3, 7, and 8, as amended herein, are respectfully traversed.

B. The Sakamoto and Gardes References

Claims 10 and 11 have been rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto and Gardes et al. (Pub. No. US 2003/0066184 A1) (Gardes). These rejections are respectfully traversed in view of the claims as amended herein.

Independent claim 10 recites a method of manufacturing a bipolar transistor comprising:

> providing a bipolar transistor including a base region, an emitter region and a metal layer providing contacts to the base region and the emitter region, the bipolar transistor having a specific area resistance of less than 500 mOhms.mm^2 when the metal layer has a thickness of less than 3μm; and
>
> increasing the thickness of the metal layer to be greater than 3μm.

Claim 10 is neither taught, suggested, nor rendered predictable by Sakamoto and Gardes, alone or in the combination suggested by the Examiner.

The Examiner cites Sakamoto, as previously described, and further cites Gardes, which as the Examiner argues, discloses "how an increasing thickness of a metal layer will result in decreases in series resistance as well as a small voltage drop (see Fig. 1, ,-r33)." *See Office Action* at Section 8.

However, Gardes does not address the distinction between claim 10 and Sakamoto at least for the reasons discussed with respect to claim 1. Furthermore, as discussed above, the benefit for which the Examiner cites Gordes is minimal. Furthermore, Gardes teaches nothing about the beneficial effect that reduced resistance has in reducing the collector-emitter saturation voltage of a low-saturation resistance bipolar transistor.

To establish a prima facie obviousness of a claim invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 490 F.2d 981 (CCPA 1974). Because none of the references disclose or suggest the recited features, there can be no prima facie obviousness by seeking to combine these references.

Therefore, for at least the reasons above, Sakamoto and Gardes do not anticipate, suggest, or render predictable independent claim 10. Claim 11 depends from claim 10 (directly or indirectly) and is allowable for at least the same reasons as claim 10 is allowable. Accordingly, the rejections of claims 10 and 11, as amended herein, are respectfully traversed.

III. New Claims:

New claims 12-14 are added to further protect additional features of the present invention.

Claim 12 generally recites,

> A bipolar transistor according to claim 2, wherein adjacent apertures are spaced less than 100μm from each other.

This claim is allowable at least for the reasons of its parent claims and/or the reasons previously discussed.

Claim 13 generally recites,

> A bipolar transistor according to claim 3, wherein adjacent apertures are spaced less than 100μm from each other.

This claim is allowable at least for the reasons of its parent claims and/or the reasons previously discussed.

Claim 14 generally recites,

> A bipolar transistor according to claim 2, wherein the thickness of the metal layer is no less than 6μm.

This claim is allowable at least for the reasons of its parent claims and/or the reasons previously discussed.

IV. Conclusion:

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 19-0741. Should no proper payment be enclosed herewith, as by the credit card payment instructions in EFS-Web being incorrect or absent, resulting in a rejected or incorrect credit card transaction, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 19-0741. If any extensions of time are needed for timely acceptance of papers submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. §1.136 and authorizes payment of any such extensions fees to Deposit Account No. 19-0741.

Respectfully submitted,

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By Michael F. Tavera No. 62,637

FOLEY & LARDNER LLP
Customer Number: 23392
Telephone: (213) 972-4594
Facsimile: (213) 486-0065

Ted R. Rittmaster
Attorney for Applicant
Registration No. 32,933